Customer No.: 31561
Docket No.: 12336-US-PA
Application No.: 10/710,662

REMARKS

Present Status of the Application

The Office Action rejected all presently-pending claims 1-18. Specifically, the Office Action rejected claims 1, 2, 6, 8-11 and 16-18 under 35 U.S.C. 102(b), as being anticipated by Sugahara (U.S. 5,401,683). The Office Action also rejected claims 3-5, 7 and 12-15 under 35 U.S.C. 103(a) as being unpatentable over Sugahara in view of Bartelink (U.S. 5,189,505).

Applicant has newly added claims 19-20. The limitation of claims 19 and 20 are described at paragraph [0025], and no new matter is entered. After entry of the foregoing amendments, claims 1-20 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

Applicant respectfully traverses the 102(b) rejection of claims 1, 2, 6, 8-11 and 16-18 because Sugahara (U.S. 5,401,683) does not teach every element recited in these claims.

In order to properly anticipate Applicants' claimed invention under 35 U.S.C 102, each and every element of claim in issue must be found, "either expressly or inherently described, in a single prior art reference". "The identical invention must be shown in as complete details as is contained in the .... claim. Richardson v. Suzuki Motor Co., 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)." See M.P.E.P. 2131, 8th ed., 2001.

The present invention is related to a stress relieving method as claim 1 recites:

Claim 1. A stress relieving method for a wafer, comprising the steps of:

providing a wafer with a dielectric layer thereon, wherein ***the wafer is divided into a first area and a second area such that at least no circuits are formed on the dielectric layer within the first area***;

forming a plurality of first openings in the dielectric layer ***within the first area***;

and

forming a first material layer over the wafer, wherein ***the upper surface of the first material layer has pits at locations over the first openings***.

Sugahara fails to disclose, teach or suggest that the wafer is divided into a first area and a second area such that at least no circuits are formed on the dielectric layer within the first area, and the upper surface of the first material layer has pits at locations over the first openings. In Sugahara's reference, as shown in Fig. 3 to Fig. 4, an oxide film 2 having openings 3 therein is formed on the substrate 1; a polysilicon layer 5 is formed over the oxide film 2; another oxide film 6 is formed over the polysilicon layer 5; a nitride film 7 is formed on the oxide film 6 above the openings 3. Next, laser beams 9 are irradiated to melt the polysilicon layer 5 from the position of opening 3 toward the position of another opening 3. After that, the polysilicon layer 5 on the oxide film 2 at ***the end of the opening 3 is recessed as a pit portion 15*** and the polysilicon layer 5 on the oxide film 2 ***at the end of the opening 3 in the downward side*** of the scanning is bulged by so much as the recess to ***form a protrusion 16***.

Sugahara does not disclose the pit portion 15 is formed within a region which no circuits are formed therein. Because in claim 1 the pits are formed within the first area with no circuits formed therein, the devices on the wafer are not affected by/from the pits. In addition, the pit portion 15 of the citation is formed at the end of the opening 3 while the protrusion 16 is formed over the end of another opening 3. The protrusion 16 is apparently different from the pit. The protrusion 16 can not relieve stress on a wafer. The pits of claim 1 are at locations over all of the

first openings and no protrusion is formed over the first openings. Besides, the pit portion 15 is formed at the end of the opening 3 but not formed above the opening 3 as claim 1 recites. Additionally, the pit portion 15 in Sugahara reference is formed from laser annealing process. However, the first openings and the pit portions of claim 1 are not formed by laser annealing. The devices on the wafers may be damaged by high temperature of laser annealing.

Therefore, Sugahara does not teach every element recited in claim 1. Applicant respectfully submits that independent claim 1 patently defines over the prior art reference, and should be allowed. For at least the same reasons, dependent claims 2-9 patently define over the prior art as well.

The present invention also provides a stress relieving method as claim 10 recites:

Claim 10. A stress relieving method for a wafer, comprising the steps of:
providing a wafer with a dielectric layer thereon, wherein ***the wafer is divided into a first area and a second area such that no circuits are formed within the first area;***
forming a first material layer over the wafer,; and
removing a portion of the first material layer within the first area to form a plurality of first openings.

Sugahara fails to disclose, teach or suggest that the wafer is divided into a first area and a second area such that no circuits are formed within the first area and removing a portion of the first material layer within the first area to form a plurality of first openings. As discussed above, Sugahara does not disclose the pit portion 15 is formed within a region which no circuits are formed therein. Because in claim 10 the first openings are formed within the first area with no circuits formed therein, the first openings do not affect the devices formed on the wafers.

Besides, in the citation the pit portion 15 is formed at the end of the opening 3 while the protrusion 16 is formed over the end of another opening 3. The protrusion 16 is apparently different from the openings. The protrusion 16 can not relieve stress on a wafer. Additionally, the pit portion 15 in Sugahara reference is formed from laser annealing process. However, the first openings of claim 10 are not formed by laser annealing. The devices on the wafers may be damaged by high temperature of laser annealing.

In addition, the Office Action points out that the step of removing a portion of the first material layer within the first area to form a plurality of first openings of claim 10 is as shown in Fig. 3 (reference 6) in Sugahara's reference. However, the reference 6 in Fig. 3 is an oxide film (col. 1, lines 50-51) but not a plurality of openings. Sugahara does not teach forming a plurality of openings in the layer 5.

For at least the foregoing reasons, Applicant respectfully submits that independent claim 10 patently defines over the prior art reference, and should be allowed. For at least the same reasons, dependent claims 11-18 patently define over the prior art as well.

Applicants respectfully traverse the rejection of claims 3-5, 7 and 12-15 under 103(a) as being unpatentable over Sugahara in view of Bartelink (U.S. 5,189,505) because a prima facie case of obviousness has not been established by the Office Action.

To establish a prima facie case of obviousness under 35 U.S.C. 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element in the claims. Second, there must be some suggestion or

motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must " be found in the prior art, and not be based on applicant's disclosure." See M.P.E.P. 2143, 8th ed., February 2003.

Applicants submit that, as discussed above, Sugahara fails to teach or suggest each and every element of claims 1, 10, from which claims 3-5, 7 and 12-15 depend. Bartelink cannot cure the deficiencies of Sugahara. Therefore, independent claims 1 and 10 are patentable over Sugahara and Bartelink. For at the least the same reasons, their dependent claims 3-5, 7 and 12-15 are also be patentable.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,

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